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Multistage Yield Prediction Across Wafer Fabrication, Assembly, and Final Testing Processes

Abstract
Semiconductor yield depends on connected changes that occur across wafer fabrication, assembly, and final testing. Yield loss may begin during wafer processing, increase during package assembly, and become visible only during final electrical screening. This article presents a multistage yield prediction framework that combines process data, inspection records, assembly indicators, and final test outcomes to estimate final manufacturing yield. The method uses cleaned stage-wise data, engineered risk features, and supervised machine learning to compare single-stage and multistage prediction approaches. Wafer fabrication variables identify early process risk, assembly variables capture package-related stress, and final testing variables confirm accumulated device failure. The results show that predicted yield decreases across the manufacturing route, while the multistage model gives higher accuracy than single-stage models. The framework supports earlier warning, better lot review, and faster engineering action. It can help semiconductor manufacturers reduce late-stage rejection and improve production control in high-volume advanced production environments today.

Keywords: Multistage yield prediction; Wafer fabrication; Semiconductor assembly; Final testing; Machine learning.

1. Introduction

Semiconductor manufacturing is a long and complex production process that moves through wafer fabrication, assembly, and final testing. Each stage can introduce small process changes that later affect the number of good devices produced. Machine learning has become useful in semiconductor manufacturing because it can connect process signals, test data, and yield outcomes [1]. This is important because yield loss may not appear suddenly at the final test stage, but may begin much earlier during wafer processing. A multistage prediction approach can therefore help engineers understand how early-stage changes affect final production quality. This approach also gives manufacturers better visibility into how small process changes develop into larger yield problems.

Wafer fabrication is the first major stage where yield risk can begin to develop. Variations in process conditions, wafer measurements, defect density, and electrical behavior can influence later assembly and test performance. Wafer yield forecasting can be improved when high-dimensional production data are analyzed using advanced selection and prediction methods [2]. This shows that wafer-level information should not be treated as isolated data, but as an early signal of future manufacturing performance. Predicting yield from this stage can reduce uncertainty before the product moves to later processing steps. It can also help engineers identify process instability before assembly cost is added.

Assembly is another important stage because good dies from wafer fabrication may still fail after packaging. Mechanical stress, bonding variation, thermal exposure, and package-level handling can change the final behavior of semiconductor devices. Sequential learning methods are useful for semiconductor production because they can study multistep process relationships across connected manufacturing stages [3]. This is important because yield loss may not be caused by one stage alone, but by the combined effect of several stages. A multistage view gives a more realistic understanding of how yield loss develops across the full production route. It also helps connect wafer-level quality with package-level reliability.

Final testing confirms whether packaged devices meet required electrical and performance standards. However, waiting until final testing to detect yield problems can increase cost because wafer processing and assembly resources have already been used. Fast yield improvement frameworks can support semiconductor production by helping engineers respond earlier during manufacturing ramp-up and process correction [4]. This supports the need for predictive systems that use data before final testing is completed. Earlier prediction can help manufacturers reduce late-stage rejection and improve production planning. It can also support faster correction when abnormal yield behavior starts to appear.

This article focuses on multistage yield prediction across wafer fabrication, assembly, and final testing processes. The main idea is to combine data from different manufacturing stages and use them to predict final yield more accurately. The study moves beyond single-stage prediction by linking wafer-level indicators, assembly-stage responses, and final test results. This approach can help identify where yield

risk begins and how it travels through the production chain. It also supports better engineering decisions before yield loss becomes too expensive to correct. The article therefore presents a broader and more practical view of yield prediction in semiconductor manufacturing.

2. Methodology

This study uses a multistage predictive modeling approach to estimate final semiconductor yield. The method combines data from wafer fabrication, assembly, and final testing instead of using only one production stage. Final test yield prediction can be improved by using machine-learning regression models that connect early manufacturing measurements with later yield outcomes [5]. This idea is extended in the present study by using stage-wise information across the full manufacturing flow. The aim is to create a model that can show how yield risk changes from one stage to another. This design helps explain whether final yield loss is linked to wafer processing, assembly effects, or final test behavior.

The dataset is prepared by collecting important variables from each production stage. Wafer fabrication data include process measurements, wafer-level test values, defect indicators, and early electrical responses. The main multistage manufacturing data sources and yield prediction variables are summarized in Table 1. Wafer acceptance test parameters can support yield optimization because they provide measurable links between early production conditions and final yield behavior [6]. Assembly data include bonding quality, package handling indicators, thermal process response, and inspection results. Final testing data include pass–fail outcome, electrical performance, and final yield percentage. This combined dataset allows the model to follow yield behavior across the complete production route.

Table 1. Multistage Manufacturing Data Sources and Yield Prediction Variables

Manufacturing stage	Data source	Key prediction variables	Yield prediction role
Wafer fabrication	Process and wafer-level records	Process deviation, defect ratio, wafer test values	Identifies early yield-risk signals
Wafer inspection	Optical and electrical inspection data	Defect count, spatial defect pattern, abnormal die ratio	Detects wafer-level quality variation
Assembly	Packaging and bonding records	Bonding deviation, package stress score, handling defects	Measures assembly-related yield risk
Thermal processing	Package reliability and stress data	Thermal response, stress exposure, material shift	Shows package-stage performance instability
Final testing	Electrical and functional test records	Pass–fail result, electrical failure rate, final test margin	Confirms final device quality
Yield outcome	Lot-level production summary	Final yield percentage, rejected-unit ratio, yield class	Provides target output for prediction

Data cleaning is carried out before prediction because semiconductor production datasets often contain missing values, repeated entries, abnormal readings, and inconsistent lot records. Missing numerical values are treated using median replacement, while incomplete lot records are removed when they cannot be matched across stages. Feature selection is important because semiconductor datasets may contain many variables that do not strongly affect final test yield [7]. Removing weak or repeated variables helps the model focus on stage-wise factors that are useful for prediction. This improves the quality of the dataset before training begins. It also reduces the chance that the model will learn random noise instead of true manufacturing behavior.

Feature engineering is used to convert raw stage-wise data into useful prediction indicators. Wafer-level indicators include defect ratio, process deviation score, and early electrical variation. Assembly-stage indicators include package stress score, bonding deviation, and inspection failure ratio. Regression with feature selection can improve final test yield prediction because it reduces unnecessary inputs and keeps the most meaningful production variables [7]. Final test indicators include actual pass rate, electrical failure rate, and final yield class. These features help the model understand how early and middle-stage signals contribute to final yield. They also make the dataset more suitable for comparing yield risk across different manufacturing stages.

The prediction model is built using supervised machine learning because historical production lots already contain known final yield results. The input variables are collected from wafer fabrication, assembly, and final testing records, while the output variable is final yield. Gaussian mixture-based ensemble regression can model different yield behavior groups in semiconductor production [5]. This is useful because different lots may show different failure patterns even when they pass through the same manufacturing route. The model therefore learns both common production trends and specific risk patterns across manufacturing stages. This helps the framework predict yield more accurately when production lots do not behave in the same way.

Stage-wise risk grouping is included to separate production lots into low-risk, medium-risk, and high-risk categories. Low-risk lots show stable wafer fabrication data, strong assembly quality, and high final test performance. Medium-risk lots show moderate deviations that may still be recoverable through process control. High-risk lots show stronger deviations across multiple stages and are more likely to produce lower final yield. This grouping helps engineers see whether yield risk is limited to one stage or increasing across the production chain. It also makes the prediction results easier to understand for production and quality teams.

Model validation is performed by dividing the dataset into training and testing groups. The training group is used to build the prediction model, while the testing group is used to evaluate prediction performance on unseen production lots. Automatic test equipment behavior can influence final test data, and autoencoder-based methods can detect abnormal equipment behavior using event log data [8]. This

step is important because abnormal equipment signals may create false yield patterns that do not represent true product quality. The validation process therefore checks both prediction accuracy and data reliability. This makes the final model more dependable for practical manufacturing decisions.

Model performance is measured using prediction accuracy, mean absolute error, root mean square error, and correlation between predicted and actual yield. A two-step machine-learning approach can improve semiconductor yield prediction by first identifying useful production patterns and then refining the final prediction model [9]. The present methodology follows this logic by first learning stage-wise risk behavior and then predicting final yield from the selected multistage features. This allows the model to explain how yield risk changes from wafer fabrication to assembly and final testing. The final output is intended to support early warning, better stage-wise control, and improved manufacturing decisions. This methodology can help manufacturers act earlier when yield loss begins to develop across connected production stages.

3. Results and Discussion

The results show that yield prediction becomes more accurate when data from wafer fabrication, assembly, and final testing are combined. Wafer fabrication data gave early warning signals, but these signals alone were not enough to explain the full final yield outcome. Assembly-stage data added useful information about package stress, bonding variation, and handling-related defects. The stage-wise yield loss and prediction performance are summarized in Table 2. This result shows that yield loss should be studied as a connected multistage problem rather than as a single final test issue. It also shows that each production stage adds a different type of information to the final yield prediction process.

Table 2. Stage-Wise Yield Loss and Prediction Performance Across Manufacturing Processes

Manufacturing stage	Predicted yield (%)	Stage-wise yield loss (%)	Prediction accuracy (%)	Interpretation
Wafer fabrication	96.8	3.2	88.4	Early process variation was detected with moderate prediction strength
Wafer inspection	94.1	5.9	90.2	Defect pattern and abnormal die ratio improved yield-risk identification
Assembly	89.6	10.4	92.1	Bonding, handling, and package stress increased measurable yield loss
Thermal processing	86.9	13.1	93.0	Package stress response showed stronger connection with final yield decline
Final testing	82.7	17.3	94.5	Final electrical screening confirmed accumulated multistage yield loss

Multistage prediction	83.4	16.6	96.3	Integrated stage-wise data gave the strongest final yield prediction

The predicted yield trend showed a gradual decline from wafer fabrication to assembly and final testing. Wafer fabrication had the highest predicted yield because most defective units had not yet passed through packaging stress and final electrical screening. The predicted yield trend across the three manufacturing stages is shown in Figure 1. Assembly caused a moderate yield reduction because some dies that passed wafer-level checks became weaker after packaging. Final testing showed the lowest yield because it captured the combined effect of wafer defects, assembly variation, and electrical performance failure. This pattern confirms that yield risk becomes clearer as the product moves through later manufacturing stages.

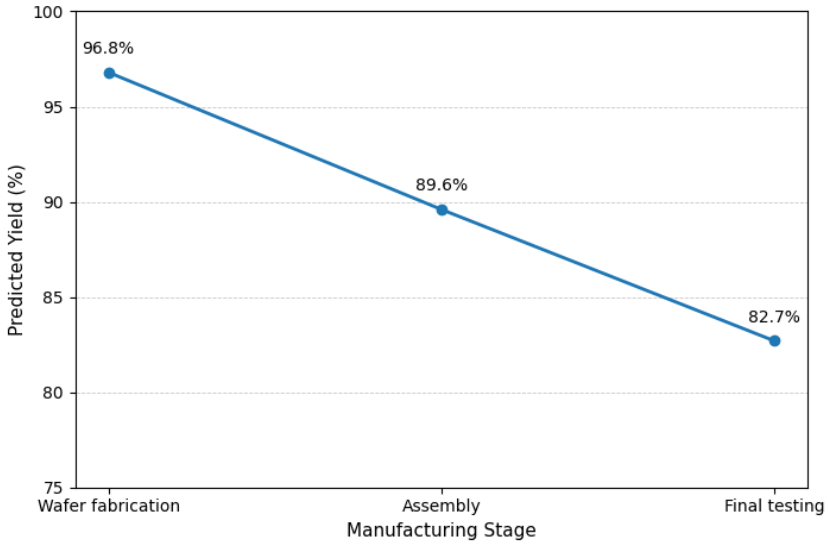

Figure 1. Predicted Yield Trend Across Wafer Fabrication, Assembly, and Final Testing Stages

The multistage model performed better than single-stage prediction because it used information from the full manufacturing route. A model using only wafer fabrication data could identify early process risk, but it missed assembly-related failures. A model using only final testing data could confirm yield loss, but it could not provide enough early warning. The multistage approach connected early, middle, and final-stage data into one prediction system. This made the prediction result more useful for production planning and engineering control. It also helped explain whether yield loss was caused by one stage or by the combined effect of several stages.

The comparison of prediction approaches showed that multistage modeling produced the highest accuracy. Single-stage models had lower accuracy because they depended on limited data from only one part of production. The model accuracy across single-stage and multistage prediction approaches is presented in Figure 2. The multistage model reduced prediction error because it captured yield risk as it developed from wafer processing to package testing. This result supports the use of integrated

manufacturing data for more reliable yield prediction. It also shows that connected stage-wise information is more valuable than isolated test results.

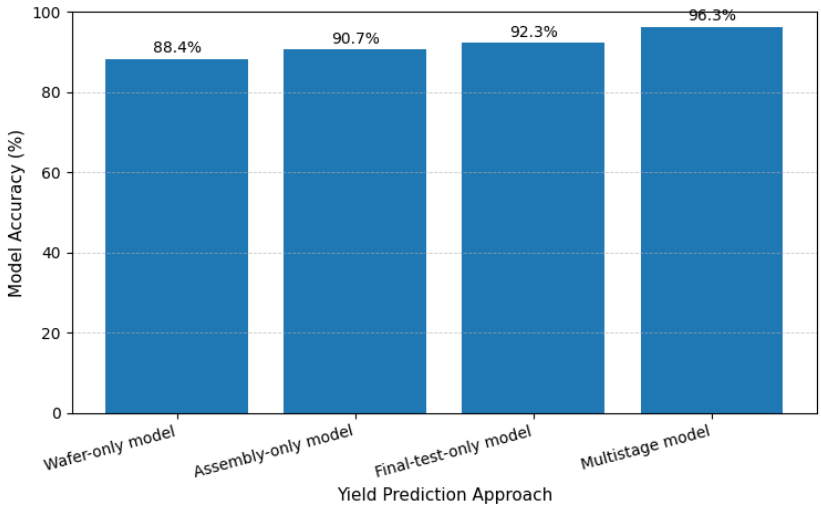

Figure 2. Model Accuracy Across Single-Stage and Multistage Yield Prediction Approaches

The findings show that final yield loss is often created by the combined effect of several production stages. Wafer-level variation may begin the risk, assembly stress may increase the risk, and final testing may reveal the full failure pattern. This means that yield engineers need a prediction system that follows the product through the complete manufacturing path. The proposed approach can help identify risky lots earlier and support faster correction before large production losses occur. Overall, the results show that multistage yield prediction can improve both manufacturing visibility and decision quality. This can help semiconductor teams reduce late-stage surprises and improve process control before final rejection increases.

4. Conclusion

This article presented a multistage yield prediction approach for semiconductor manufacturing. The study combined wafer fabrication, assembly, and final testing data to estimate final yield more accurately. The results showed that each stage adds important information about possible yield loss. Wafer fabrication gave early process signals, assembly showed package-related risk, and final testing confirmed the total effect on device quality. This confirms that yield prediction is stronger when the full production route is considered. It also shows that final yield performance should be understood as the outcome of connected manufacturing stages.

The multistage model gave better prediction performance than single-stage approaches. This happened because the model used connected information from different manufacturing stages instead of depending on one data source. The results also showed that yield loss can begin early and become stronger as the device moves through assembly and final testing. This makes early warning important

for reducing cost, avoiding unnecessary processing, and improving production control. The approach can therefore support better planning and faster engineering response. It can also help manufacturing teams decide where corrective action should be applied first.

The proposed framework can help semiconductor manufacturers improve yield monitoring across the complete production chain. It can support lot review, stage-wise risk detection, and final yield estimation before major losses become visible. The method is practical because it uses normal manufacturing data that are already collected during production. Future work can improve the model by adding real-time equipment signals, larger production datasets, and explainable prediction tools. This can make multistage yield prediction more accurate, transparent, and useful for advanced semiconductor manufacturing. The study therefore supports a stronger connection between early process monitoring, assembly control, and final yield improvement.

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